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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/398,189	09/17/99	KANAMORI	J IIZ.008D

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MMC1/0718

EXAMINER	
RAO, S	
ART UNIT	PAPER NUMBER

2814

DATE MAILED: 07/18/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.
09/398,189

Applicant(s)
Jun Kanamori

Examiner
S.H. Rao

Group Art Unit
2814



☒ Responsive to communication(s) filed on Sep 17, 1999

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 35 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) 1-9 is/are pending in the applicant

Of the above, claim(s) _____ is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 1-9 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

— SEE OFFICE ACTION ON THE FOLLOWING PAGES —

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DETAILED ACTION

Information Disclosure Statement

The IDS was filed without enclosing the cited document because it was also cited in the parent case. Attempts to locate the parent case by the Examiner were unsuccessful. The examiner contacted Mr. Adam Voltentine to try to obtain a second copy, which the Examiner has not received to date, therefore the IDS and the single reference contained therein has not been considered. The IDS will be considered and the 1449 duly initialed when a copy of the reference is available to the Examiner.

Claim Rejections - 35 U.S.C. § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants' Applicants' admitted prior art.

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3. In re Claim 1, Applicants' admitted prior art (conventional method described on pages 2-4 of the instant specification) teaches a method of making a semiconductor device by a self aligned silicide process including the steps of :

providing a material to be silicided at least on the surface of an area to be silicided (Specification page 2 lines 7-9) ; a first RTA to form a first- reacted silicide region (Specification page 2 lines 9-12); and performing a second RTA to form a second-reacted silicide region (Specification page 2 lines 16-20).

Applicants' admitted prior art does not specifically teach for providing a supplemental silicon layer over the surface.

However, Applicants' admitted prior art at page 2 lines 16-18 teaches the removing of metal by wet etching to expose silicon which is then silicided by a second RTA in order to ensure that incomplete silicide are not present after the first RTA and to provide an silicide region having a desired low resistance.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to provide supplemental silicon instead of wet etching to expose the silicon which is then silicided by a second RTA in order to ensure that incomplete silicide are not present after the first RTA and to provide an silicide region having a desired low resistance.(Specification page 2 line 18-19).

In re claims 2 and 3, applicants' admitted prior art page line 8, teaches material to be cobalt or titanium.

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In re claim 4, forming a polysilicon layer by CVD is well known in the art.

Claims 5-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants'

Applicants' admitted prior art and Burgener (U.S. Patent No. 5,863,823 , herein after Burgener).

In re claims 5 and 6 , Applicants' admitted prior art teaches a method of making a semiconductor device by a self aligned silicide process, including selectively removing non-reacted silicon after RTA. (The unreacted silicon will be removed during the wet etch and removing unreacted silicon after the first RTA as stated in the back ground art is not patentably distinct from removing it after second RTA).

Applicants' admitted prior art does not specifically teach the supplemental silicon layer to be amorphous silicon formed by sputtering.

However, Burgener in col. 4 lines 28 teaches an amorphous silicon film by sputter deposition so that uniform amorphization can be achieved in subsequent processing steps.

Therefore, it would have been obvious to one of ordinary skill in the art , at the time of the invention to substitute the silicon of Applicants' admitted prior art with Burgener's amorphous silicon formed by sputter deposition in order to achieve uniform amorphization in subsequent processing steps.

In re Claims 7 and 8, Burgener at col. 6 lines 4 thru' lines 10 teaches doping impurities in to N and P channel.

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In re Claims 9, Applicants' admitted prior art at page 2 line 1 teaches the formation of BOX layer, the rest of the steps recited in claim 9 are a repeat of the earlier recited steps in claims 1-8.

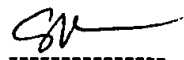
Conclusion

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Steven H. Rao whose telephone number is (703) 306-5945. The fax number is (703) 308-7722 or -7724. The Examiner can be normally reached on Monday-Friday from 9.30 a.m. to 6.00 p.m. (EST).

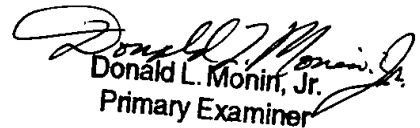
If attempts to reach the examiner by telephone are unsuccessful, the examiner's Supervisor Ex. Olik Chaudhuri, can be reached at (703) 306-2794.

Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission at the above mentioned fax numbers.

Any inquiry of a general nature or relating to the status of this application should be directed to the Technology center 2800 receptionist at (703) 308-0956.



July 13, 2000.


Donald L. Monir, Jr.
Primary Examiner